CLAIMS

1. A controller comprising:
a logic core having a plurality of inputs and a plurality of outputs; and
a memory;
wherein the controller functions as a state machine and upon the transition from a state to a succeeding state the operation of the logic core is modified in accordance with data held in the memory.

2. A controller as claimed in claim 1, in which the logic core represents a state having up to three outputs.

3. A controller as claimed in claim 1, in which the logic core includes a fault detector.

4. A controller as claimed in claim 3, in which the fault detector has a plurality of inputs and a lesser number of outputs.

5. A controller as claimed in claim 4, in which the fault detector has a single output.

6. A controller as claimed in claim 4, in which at least one input of the fault detector is associated with a respective input detector which is responsive to at least one of:
   a) a mask/select control signal for determining whether an input signal at a signal input of the input detector should be taken into consideration by the fault detector; and
   b) an invert signal for causing an output signal from the input detector to be inverted with respect to the input signal.

7. A controller as claimed in claim 4, in which at least one input detector has multiple signal inputs and it is responsive to the order in which the signal inputs change.

8. A controller as claimed in claim 3, in which the fault detector includes combinational logic for combining its inputs in a logical OR.

9. A controller as claimed in claim 5 in which an output of the fault detector is supplied to a device arranged in a first mode to pass the output of the fault detector in a non-inverted state and in a second mode to invert the output of the fault detector.

10. A controller as claimed in claim 1 in which the logic core includes a combinational logic unit having a plurality on inputs and a single output, and wherein at least one of the inputs is selectively maskable and invertable such that the combinational logic unit can be arranged to look for the occurrence of a plurality of input signals being in a predetermined state, and to assert a first predetermined output signal when the input signals are in the predetermined state and a second predetermined output signal when the input signals are not in the predetermined state.

11. A controller as claimed in claim 1 in which the logic core comprises a sequence detector.

12. A controller as claimed in claim 11, wherein the sequence detector has a plurality of inputs and a lesser number of outputs.

13. A controller as claimed in claim 12, in which the sequence detector has a single output.

14. A controller as claimed in claim 12, in which the sequence detector comprises a multiplexer responsive to a selection control word to select only one of the plurality of inputs.

15. A controller as claimed in claim 11 in which the sequence detector includes a device arranged in a first mode to pass a signal to or from the multiplexer in a non-inverted state and in a second mode to invert the signal.

16. A controller as claimed in claim 11 in which the sequence detector further includes a sequence timer arranged to assert an output signal only when an input condition monitored by the sequence detector has been in a predetermined state for a predetermined period.

17. A controller as claimed in claim 16, in which the sequence timer is programmable.

18. A controller as claimed in claim 1, in which the logic core comprises a time out circuit having a time out timer selectively arranged to assert an output a predetermined period after the logic core has entered a state.

19. A controller as claimed in claim 18, in which the time out timer is programmable.

20. A controller as claimed in claim 1, in which the memory is programmable.

21. A controller as claimed in claim 20, in which the memory is user programmable.

22. A controller as claimed in claim 20 in which the memory is non-volatile.

23. A controller as claimed in claim 1, in which the memory holds data which is a state control word comprising a least one of the following items:

a) output data defining the condition of at least one output upon entry into a state;

b) data for controlling a fault detector, and in particular data defining whether an input of the fault detector is to be masked and data identifying the next state to be executed if a fault condition is determined by the fault detector, and

c) data for controlling a sequence detector, and in particular data defining which input of the sequence detector is to be monitored and data identifying the next state to be executed if the sequence detector determines that a condition it is monitoring is satisfied.

24. A controller as claimed in claim 23, in which the memory further includes data for setting a duration timed by a time out timer and data identifying the next state to be executed after the time out timer has timed out and triggered a state change.

25. A power supply controller comprising a controller as claimed in claim 1.

26. An integrated circuit including a controller as claimed in claim 1.